Claims

What is claimed is:

1. A memory system, comprising:

a first storage device;

at least one additional storage device;

a control storage device to store a programmable indicator identifying the manner in which the first and the at least one additional storage device are to be referenced; and

a control circuit coupled to the first storage device, the at least one additional storage device, and the control storage device, the control circuit to receive a request for data, wherein the data may be stored within at least one of the first or the at least one additional storage device, and in response thereto, to initiate at least one of a first reference to the first storage device and a second reference to the at least one additional storage device in a manner controlled by the state of the programmable indicator

2. The system of Claim 1, wherein the first and the second references are issued in a time order that is controlled by the state of the programmable indicator.

3. The system of Claim 1, wherein if the programmable indicator is in a first state, the second reference is issued only if the first reference is not capable of completing the request.

4. The system of Claim 3, wherein if the programmable indicator is in a second state, the second reference is issued regardless of whether the second reference is required to complete the request.

5. The system of Claim 4, wherein if the programmable indicator is in the second state, the second reference is issued before the first reference.

6. The system of Claim 1, and further including mode switch logic to modify the state of the programmable indicator between the first state and the second state based on programmable criteria.

7. The system of Claim 6, wherein the control circuit receives multiple requests for data, and wherein the mode switch logic includes a circuit to modify the state of the programmable indicator from the first state to the second state if at least a first predetermined number of the multiple requests requires the second reference to complete.

8. The system of Claim 7, wherein the mode switch logic includes a circuit to modify the state of the programmable indicator from the second state to the first

state if a second predetermined number of the multiple requests does not require the second reference to complete

9. The system of Claim 8, wherein the mode switch logic includes a circuit that allows at least one of the first and the second predetermined numbers to be programmably selected.

10. The system of Claim 8, and further including a main memory coupled to the first storage device to issue the request to the control circuit.

11. The system of Claim 10, wherein the request is requesting data associated with one or more incomplete memory coherency actions, and further comprising a request tracking circuit coupled to the control circuit to track the incomplete memory coherency actions, whereby the data is returned to the main memory only after all of the coherency actions are completed.

12. A memory system, comprising:

first memory logic;

at least one other memory;

a storage device coupled to the first memory logic to store a programmable indicator identifying a mode of referencing the first memory logic and the at least one other memory; and

a control circuit coupled to the first memory logic and the at least one other memory, the control circuit to receive a request for data, and in response thereto, to retrieve the requested data from at least one of the first memory logic and the at least one other memory in a manner determined by the identified mode.

13. The system of Claim 12, wherein the first memory logic includes at least one of a tag memory and a memory to store data.

14. The system of Claim 12, wherein the control circuit includes a circuit to determine whether the programmable indicator is in a first predetermined state, and if so, to further determine whether the at least one other memory must be referenced to complete the request, and if not, to obtain the data from the first memory logic without reference to the at least one other memory.

15. The system of Claim 14, wherein the control circuit includes a circuit to initiate references to both the first memory logic and the at least one other memory if the at least one other memory must be referenced to complete the request.

16. The system of Claim 12, wherein the control circuit includes a circuit to determine whether the programmable indicator is in a second predetermined state, and if so, to initiate a reference to the first memory logic and the at least one other memory irrespective of whether a reference to the at least one other memory is necessary to complete the request.

17. The system of Claim 12, wherein the control circuit includes a circuit to determine if the programmable indicator is in a third predetermined state indicating the first memory logic is unavailable for storing data, and if so, to initiate a reference to the at least one other memory without attempting to obtain the requested data from the first memory logic.

18. The system of Claim 12, wherein the first memory logic includes a shared cache, wherein the at least one other memory includes one or more dedicated caches, and further comprising at least one instruction processor coupled to the one or more dedicated caches

19. The system of Claim 12, and further comprising a main memory coupled to the first memory logic to issue the request for the data.

20. The memory system of Claim 12, and further including mode switch logic coupled to the storage device to automatically re-program the programmable indicator.

21. The memory system of Claim 20, wherein the mode switch logic includes a circuit to monitor conditions within the memory system, and to automatically re-program the programmable indicator based on the monitored conditions.

22. A method for use in a data processing system having a first memory coupled to at least one other memory and a programmable storage device to identify a reference mode to control the manner in which data is retrieved from at least one of the first memory and the at least one other memory, the method comprising:

a.) receiving a request for data; and

b.) initiating an operation to retrieve data from at least one of the first memory or the at least one other memory in a manner that is determined by the reference mode.

23. The method of Claim 22, wherein step b.) comprises:

if the reference mode selects a first mode, determining whether the request can be completed without accessing the at least one other memory; and

if the request can be completed without accessing the at least one other memory, obtaining the requested data from the first memory.

24. The method of Claim 22, wherein step b.) comprises:

if the reference mode selects a first mode, determining whether the request can be completed without accessing the at least one other memory; and

if the request cannot be completed without accessing the at least one other memory, initiating references to the first memory and the at least one other memory to complete the request.

25. The method of Claim 22, wherein if the reference mode selects a second mode, initiating a reference to the first memory and the at least one other memory irrespective of which of the first memory or the at least one other memory stores the data.

26. The method of Claim 22, wherein step b.) comprises:

determining that the first memory is unavailable to store the requested data; and

obtaining the requested data from the at least one other memory.

27. The method of Claim 22, and further including modifying the reference mode based on conditions within the data processing system.

28. The method of Claim 22, wherein the data processing system includes a main memory coupled to the first memory, and wherein step a.) includes receiving a request for data from the main memory.

29. The method of Claim 22, wherein the at least one other memory includes multiple coupled memories, and wherein step b.) comprises:

issuing a request for the requested data to the multiple coupled memories; and

receiving the requested data from one of the multiple coupled memories.

30. A data processing system, comprising:

main memory means for storing data;

first cache means for storing a first sub-set of the data;

second cache means for storing a second sub-set of the data;

programmable storage means for storing one or more control signals to control the way in which data is retrieved from the first cache means and the second cache means; and

control means for receiving requests for data from the main memory, the control means further for initiating a reference to one or both of the first and second cache means based, at least in part, on the state of the one or more control signals.

31. The system of Claim 30, and further including mode switch means for monitoring system conditions and automatically altering one or more of the control signals based on the system conditions.

32. The system of Claim 30, wherein the first cache means includes tag means for storing tag information describing the first sub-set of the data; and wherein the control means includes means for initiating a reference to one or both of the first and the second cache means based, at least in part, on tag information for the requested data.